NONVOLATILE MEMORY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a nonvolatile memory device, and more specifically, to a programmable nonvolatile logic switch memory (register) using a resistive memory device.

2. Description of the Prior Art

[0002] Generally, nonvolatile memory such as magnetic memory and phase change memory (PCM) has a data processing speed similar to that of volatile RAM (Random Access Memory). When power is off, data of the nonvolatile memory are preserved.

[0003] Fig. 1 is a circuit diagram illustrating a conventional volatile logic switch device. Since conventional logic switch and register devices are volatile, data stored in such registers are not preserved when power is off.

[0004] A volatile logic switch SW1 connects a node B with a node C in response to a control signal applied to a gate input terminal A. The gate input terminal A of the volatile logic switch SW1 has no memory device for storing previous and current data. As a result, data stored in the memory device are not preserved when power is off.

[0005] Fig. 2 is a circuit diagram illustrating a

conventional flip-flop volatile memory device which is a SRAM (Static Random Access Memory).

[0006] The flip-flop volatile memory device comprises a flip-flop unit including PMOS transistors P1 and P2, and NMOS transistors N1 and N2. The flip-flop volatile memory device further comprises NMOS transistors N3 and N4 for storing data applied from bitlines BIT and /BIT in the flip-flop unit depending on an enable state of a wordline WL.

[0007] The conventional flip-flop volatile memory device can store data in both terminals of the flip-flop unit with a static state when power is on. However, the data stored in the terminals both of the flip-flop unit are destroyed when power is off.

[0008] Nonvolatile memory devices have been developed to overcome the above problem of the conventional volatile memory device. Figs. 3a to 3d are diagrams illustrating a conventional phase change memory (PCM) device.

[0009] The PCM device 4 comprises a phase change layer (PCL) 2 of phase change material for receiving voltage and current between a top electrode 1 and a bottom electrode 3. The voltage and current induce high temperature in the PCL 2, thereby changing electric conductivity of the PCL 2.

[0010] As shown in Fig. 3c, if low current of less than a

threshold value flows in the PCM device 4, the PCL 2 has a proper temperature to be crystallized. Thus, the PCL 2 comes to have high resistance.

[0011] Referring to Fig. 3d, if high current of more than a threshold value flows in the PCM device 4, the PCL 2 has a temperature over a melting point of the phase change material. Thus, the PCL 2 becomes uncrystallized to have low resistance.

[0012] The PCM device 4 can store nonvolatile data corresponding to the two resistances.

SUMMARY OF THE INVENTION

[0013] Accordingly, it is an object of the present invention to provide a programmable nonvolatile logic switch memory (register) device using a nonvolatile resistance memory device.

[0014] In an embodiment, there is provided a nonvolatile memory device comprising a write/read controller, a nonvolatile resistive memory device and a logic switch. The write/read controller selectively controls write/read control signals enabled in a write mode. As used herein, a nonvolatile resistive memory device is a circuit element that stores different logic values in the level of electrical resistance of one or more circuit elements, such that the states of resistance of the element or elements can be changed or set (e.g., set to a high resistance or set to a low resistance) by

controlling the amount of current that passes through the device when the write/read control signals are enabled. The logic switch selects switching states depending on the different logic values pre-stored in the nonvolatile resistive memory device when the write/read control signals are disabled.

[0015] In an embodiment, there is also provided a nonvolatile memory device comprising a flip-flop unit, a nonvolatile resistive memory device, an access controller and a current supply unit. The flip-flop unit includes a PMOS latch and a NMOS latch, and latch the opposite data. The nonvolatile resistive memory device, which is connected between the PMOS latch and the NMOS latch, stores different logic values depending on states of resistance changed by the amount of current. The access controller controls connection of a bitline and the flip-flop unit depending on an enable state of a wordline. The current supply unit supplies current for changing data stored in the resistive memory device when the write/read control signals are enabled.

[0016] In an embodiment, there is also provided a nonvolatile memory device comprising a flip-flop unit, a nonvolatile resistive memory device and an access controller. The flip-flop unit includes a NMOS latch for latching opposite data. The nonvolatile resistive memory device, which is connected between a power voltage terminal and the flip-flop

unit, stores different logic values depending on states of resistance changed by the amount of current. The access controller controls a connection of a bitline to the flip-flop unit depending on an enable state of a wordline.

[0017] In an embodiment, there is provided a nonvolatile memory device comprising a flip-flop unit, an access controller and a nonvolatile resistive memory device. The flip-flop unit includes a NMOS latch for latching opposite data. The access controller controls a connection of a bitline to the flip-flop unit depending on an enable state of a wordline. The nonvolatile resistive memory device, which is connected between the flip-flop unit and the access controller, stores different logic values depending on states of resistance changed by the amount of current.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Fig. 1 is a circuit diagram illustrating a conventional volatile logic switch device.

[0019] Fig. 2 is a circuit diagram illustrating a conventional flip-flop volatile memory device.

[0020] Figs. 3a to 3d are diagrams illustrating a conventional PCM device.

[0021] Figs. 4a and 4b are circuit diagrams illustrating a

nonvolatile memory device according to an embodiment of the present invention.

[0022] Figs. 5 to 9 are circuit diagrams illustrating a nonvolatile memory device according to other embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023] The present invention will be described in detail with reference to the attached drawings.

[0024] Fig. 4a is a circuit diagram illustrating a nonvolatile memory device used as a nonvolatile logic switch according to an embodiment of the present invention.

[0025] In an embodiment, the nonvolatile memory device comprises a write/read controller 20, resistance memory devices R1 and R2, and a logic switch SW2.

[0026] The write/read controller 20 selectively outputs a write/read control signal WRC1 in response to a write control signal WRC2 inputted into a gate of a NMOS transistor N5 and a write control signal WRC3 inputted into a gate of a PMOS transistor P3. The write control signal WRC2 has an opposite phase to that of the write control signal WRC3.

[0027] The resistive memory device R1 is connected between a node D and a node F. The resistive memory device R2 is

connected between a node E and a node F. The node F is connected to a gate of the logic switch SW2.

[0028] Next, the write operation according to an embodiment of the present invention is described.

[0029] When the write control signal WRC2 inputted in the write/read controller 20 is at a high level, the NMOS transistor N5 is turned on. When the write control signal WRC3 is at a low level, the PMOS transistor P3 is turned on, and the write/read control signal WRC1 is outputted.

[0030] If current is applied between the nodes D and F, data is written in the resistive memory device R1. If current is applied between the nodes E and F, data is written in the resistive memory device R2.

[0031] The resistive memory devices R1 and R2 of Fig. 4a may be represented like those in Fig. 4b.

[0032] When the write control signal WRC2 is at a low level and the write control signal WRC3 is at a high level, the NMOS transistor N5 and the PMOS transistor P3 of the write/read controller 20 are all turned off. Here, when the resistive memory device R1 has a low resistance and the resistive memory device R2 has a high resistance, the states of the logic switch SW2 are determined depending on states of input signals through the input nodes D and E.

[0033] Table 1 shows the operation of the logic switch SW2 depending on input signals when low data is stored in the resistive memory device R1 and the high data is stored in the resistive memory device R2.

[TABLE 1]

D	E	R1	R2	SW2
L	L	L	H	OFF
H	L	L	H	ON
L	H	L	H	OFF
H	H	L	H	ON

[0034] When a high level signal is applied to the node D and a high or low level signal is applied to the node E, the logic switch SW2 is turned on to output a signal of the node ND1 into the node ND2.

[0035] On the other hand, when a low level signal is applied to the node D and a low or high level signal is a applied to the node E, the logic switch SW2 is turned off. As a result, the signal of the node ND1 is not outputted into the node ND2.

[0036] When the resistive memory device R1 has a high resistance and the resistive memory device R2 has a low resistance, the states of the logic switch SW2 are determined depending on states of input signals inputted through the input nodes D and E.

[0037] Table 2 shows the operation of the logic switch SW2 depending on the input signals when high data is stored in the

resistive memory device R1 and low data is stored in the resistive memory device R2.

[TABLE 2]

D	E	R1	R2	SW2
L	L	H	L	OFF
H	L	H	L	OFF
L	H	H	L	ON
H	H	H	L	ON

[0038] When a high or low level signal is applied to the node D and a high level signal is applied to the node E, the logic switch SW2 is turned on to output a signal of the node ND1 into the node ND2.

[0039] When the high or low level signal is applied to the node D and a low level signal is applied to the node E, the logic switch SW2 is turned off. As a result, the signal of the node ND1 is not outputted into the node ND2.

[0040] Fig. 5 is a circuit diagram illustrating a nonvolatile memory device used as a nonvolatile logic register according to other embodiment of the present invention.

[0041] In an embodiment, the nonvolatile memory device comprises a flip-flop unit 30, resistive memory devices R3 and R4, an access controller including NMOS transistors N8 and N9, and a current supply unit including PMOS transistors P6 and P7.

[0042] The flip-flop unit 30 comprises a NMOS latch including NMOS transistors N6 and N7, and a PMOS latch

including PMOS transistors P4 and P5. The NMOS latch and the PMOS latch store opposite data.

[0043] The resistive memory device R3, which is connected to a common drain of the PMOS transistor P4 and the NMOS transistor N6, stores nonvolatile data. The resistive memory device R4, which is connected to a common drain of the PMOS transistor P5 and the NMOS transistor N7, stores nonvolatile data.

[0044] The access controller, including the NMOS transistors N8 and N9, controls a connection of bitlines BIT and /BIT depending on an enable state of a wordline WL. The NMOS transistor N8 having a gate connected to the wordline WL is connected between the bitline BIT and the drain of the NMOS transistor N6. The NMOS transistor N9 having a gate connected to the wordline WL is connected between the bitline /BIT and the drain of the NMOS transistor N7.

[0045] The current supply unit comprises PMOS transistor P6 and P7 for changing data stored in the resistive memory devices R3 and R4 in a write mode. The PMOS transistor P6 connected in parallel to the PMOS transistor P4 has a gate to receive a write/read control signal WRC. The PMOS transistor P7 connected in parallel to the PMOS transistor P5 has a gate to receive the write/read control signal WRC.

[0046] Gate input signals of the PMOS latch and the NMOS

latch are connected to the resistive memory devices R3 and R4 with a positive feedback type circuit.

[0047] When the write/read control signal WRC is at a low level, the PMOS transistors P6 and P7 are turned on to apply a predetermined voltage to the bitlines BIT and /BIT. Then, a difference in current flowing in the resistive memory devices R3 and R4 is generated by a difference in voltages of the bitlines BIT and /BIT. As a result, the amount of heat applied to the resistive memory devices R3 and R4 is also differentiated.

[0048] Here, voltages of the bitlines BIT and /BIT are determined to generate heat in the resistive memory devices R3 and R4 over or below the melting point.

[0049] Fig. 6 is a circuit diagram illustrating a nonvolatile memory device according to other embodiment of the present invention.

[0050] The embodiment shown in Fig. 6 is different from that of Fig. 5 in that gate input signals of the PMOS latch P4,P5 and the NMOS latch N6,N7 are connected to the resistive memory devices R3 and R4 with a negative feedback type circuit. The explanation of the rest configuration and operation is omitted because it is similar to that of Fig. 5.

[0051] Fig. 7 is a circuit diagram illustrating a

nonvolatile memory device according to another embodiment of the present invention.

[0052] In this embodiment, the nonvolatile memory device comprises a flip-flop unit 30, resistive memory devices R3 and R4, an access controller including NMOS transistors N8 and N9, and a driver which is a NMOS transistor N10.

[0053] The flip-flop unit 30 comprises a NMOS latch including NMOS transistors N6 and N7. Gate input signals of the NMOS transistors N6 and N7 are connected to the resistive memory devices R3 and R4 with a positive feedback type circuit.

[0054] The resistive memory device R3, which is connected to a common drain of the NMOS transistors N6 and N10, stores nonvolatile data. The resistive memory device R4, which is connected to a common drain of the NMOS transistors N7 and N10, stores nonvolatile data.

[0055] The access controller comprises NMOS transistors N8 and N9 for controlling connection of bitlines BIT and /BIT depending on an enable state of a wordline WL. The NMOS transistor N8 having a gate connected to the wordline WL is connected between the bitline BIT and a drain of the NMOS transistor N6. The NMOS transistor N9 having a gate connected to the wordline WL is connected between the bitline /BIT and a drain of the NMOS transistor N7.

[0056] The driver comprises a NMOS transistor N10. The NMOS transistor N10, connected between a power voltage VCC terminal and the resistive memory devices R3 and R4, has a gate to receive a write/read control signal WRC.

[0057] Fig. 8 is a circuit diagram illustrating a nonvolatile memory device according to another embodiment of the present invention.

[0058] In the nonvolatile memory device of Fig. 8, gate input signals of NMOS transistors N6 and N7 are connected to resistive memory devices R3 and R4 with a negative feedback type circuit. The nonvolatile memory device of Fig. 8 does not comprise a NMOS transistor N10 like that of Fig. 7. The explanation of the rest configuration and operation is omitted because it is similar to that of Fig. 7.

[0059] Fig. 9 is a circuit diagram illustrating a nonvolatile memory device according to another embodiment of the present invention.

[0060] The nonvolatile memory device of Fig. 9 comprises a flip-flop unit 30, resistive memory devices R3 and R4, and an access controller including NMOS transistors N8 and N9.

[0061] The flip-flop unit 30 comprises a NMOS latch including NMOS transistors N6 and N7. Gate input signals of the NMOS transistors N6 and N7 are connected to the resistive

memory devices R3 and R4 with a positive feedback type circuit.

[0062] The resistive memory device R3, connected between a terminal of the NMOS transistor P8 and a drain of the NMOS transistor N6, stores nonvolatile data. The resistive memory device R4, connected between a terminal of the NMOS transistor P9 and a drain of the NMOS transistor N7, stores nonvolatile data.

[0063] The access controller including the NMOS transistors N8 and N9 controls a connection of bitlines BIT and /BIT depending on an enable state of a wordline WL. The NMOS transistor N8 having a gate connected to the wordline WL is connected between the bitline BIT and a terminal of the resistive memory device R3. The NMOS transistor N9 having a gate connected to the wordline WL is connected between the bitline /BIT and a terminal of the resistive memory device R4.

[0064] Although a PCM device is exemplified as a resistive memory device in the above embodiments, a MTJ (Magnetic Tunneling Junction) or GMR (Giant Magnetic Resistive) device can be used as a resistive memory device alternatively.

[0065] Additionally, a nonvolatile memory device according to an embodiment of the present invention can be utilized as a nonvolatile programmable gate memory device such as a FPGA (Field Programmable Gate Array).

[0066] As discussed earlier, a nonvolatile memory device can be embodied using a resistive memory device in an embodiment of the present invention. Such a programmable register is applied to a memory chip in order to program data for regulating redundancy and reference with a software type, thereby improving reliability of the chip.

[0067] While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and described in detail herein. However, it should be understood that the invention is not limited to the particular forms disclosed. Rather, the invention covers all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined in the appended claims.